

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 06-045606

(43)Date of publication of application : 18.02.1994

(51)Int.Cl.

H01L 29/784
G02F 1/136

(21)Application number : 04-195040

(71)Applicant : FUJITSU LTD

(22)Date of filing : 22.07.1992

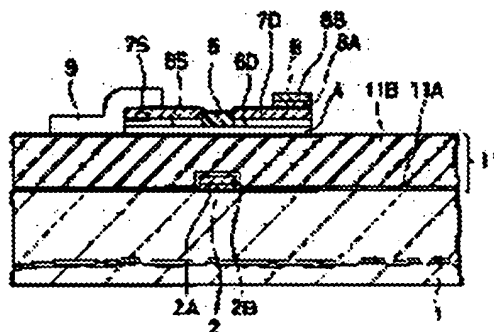
(72)Inventor : KOSUGI KIYOHISA
WATABE JUNICHI

(54) MANUFACTURE OF THIN-FILM TRANSISTOR MATRIX

(57)Abstract:

PURPOSE: To obtain a good TFT characteristic wherein a gate dielectric withstand voltage is not lowered even when a gate electrode composed of Al or a gate bus line is combined with a gate insulating film composed of an Al₂O₃ ALD film regarding the manufacturing method of a thin-film transistor matrix.

CONSTITUTION: A gate electrode 2 at least the surface of which is constituted of Al and a gate bus line are formed on a transparent insulating substrate 1, a metal film having a thickness capable of being changed into an insulator by oxidation is formed, the metal film is oxidized inside an atomic-layer deposition film formation apparatus or the metal film is oxidized inside an oxygen plasma ashing apparatus and the metal film is changed into an insulating metal oxide film. Then, an Al₂O₃ film 11B is laminated on it by an atomic-layer deposition method, a gate insulating film 11 is formed and, after that, an active semiconductor layer 4, a source electrode 7S, a drain electrode 7D, a drain bus line 8 and a pixel electrode 9 are formed sequentially.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]